University of Bahrain
College of Information technology
Department of Computer Engineering

Test (2)

Student Name	
I.D. No.	
Section	

Course Title: Digital Logic
Course number: ITCE 202-250
Semester: 1
Academic Year: 2014/2015
Duration : 1 hour
Date: 9th December 2014

Read the following before you start:

1. **Write with PEN**
2. Write your name, ID and section number
3. Answer all questions.
4. Write your answers on the attached sheets only.

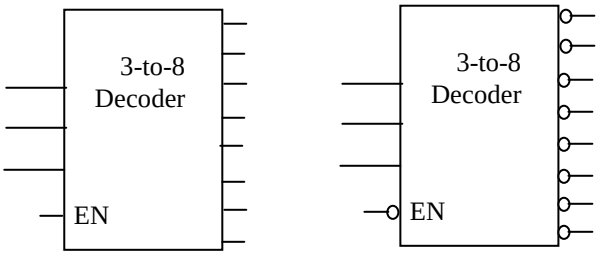
Question	Mark
1 (20 Mark)	
2 (18 Mark)	
3 (20 Marks)	
4 (18 Mark)	
5 (24 Mark)	
Total (100)	

Question [1]: (20 Mark)

Implement the following Boolean function:

$$f(A,B,C) = \Sigma m(0,3,4,7)$$

Using a 3-to-8 line decoder and:



a. an extra OR gate.

b. an extra NAND gate.

c. an extra AND gate.

d. an extra NOR gate.

Question [2]: (18 Marks)

Implement the following function with a 4-to-1 Multiplexer and a minimum number of logic gates:

$F(a,b,c,d) = \Sigma m(,0,1,4,7,8,9,10,15,)$

Question [3]: (20 Marks)

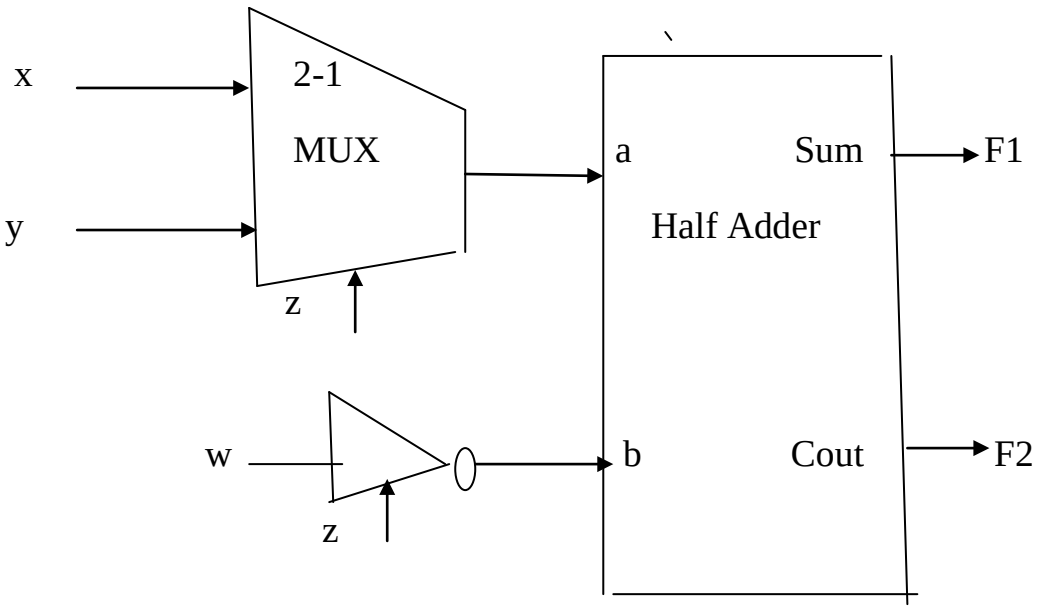
A ROM that stores the values of the following arithmetic function is to be designed:

F= 2(a+b) where a and b are 2-bit binary numbers.

a- Give the size of the ROM

b- Draw the internal structure of the ROM showing the last 3 memory lines.

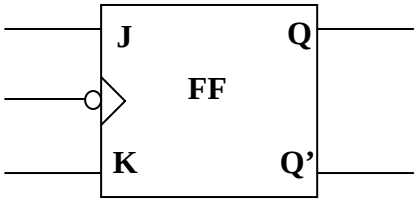
Question [4]: (18 Marks)

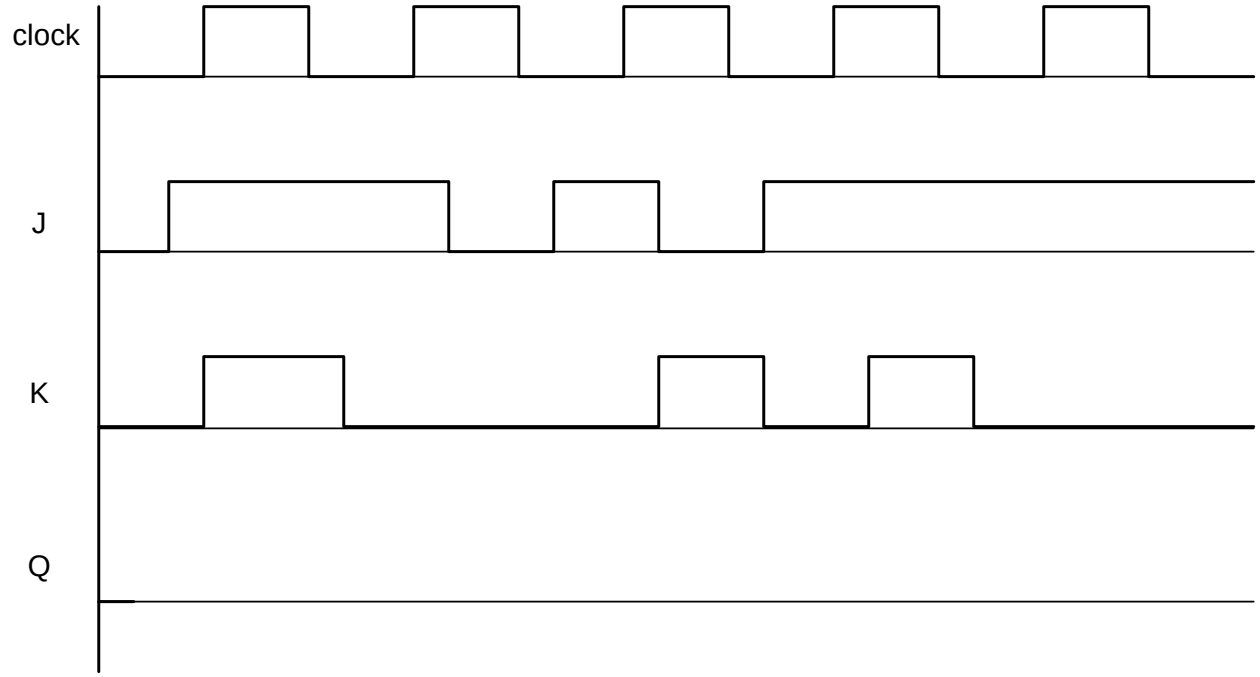


Write the equations of the inputs a and b of the given Half Adder, then give the equations of F1 and F2.

Question [5]: (24 Marks)

a. Complete the timing diagram for the given Flip-Flop. (Assume the initial state of the F-F is equal to zero).





b. Convert a J-K to S-R Flip-Flop showing all steps.